*FIG. 2*

*FIG. 2*

```

    graph TD
        ROM[ROM] --- MC[MOTOR CONTROL]
        ROM --- RWC[READ/WRITE CONTROL]
        ROM --- ACT[ACT CONTROL]
        MC --- RWC
        RWC --- ACT
        subgraph PCB [PCB]
            ROM
            MC
            RWC
            ACT
            subgraph RAM [RAM]
                RAM1[RAM]
                RAM2[RAM]
            end
            subgraph μP [μP]
                μP1[μP]
                μP2[μP]
            end
        end
        RWC --- Head[Head Assembly]
    
```

FIG. 3

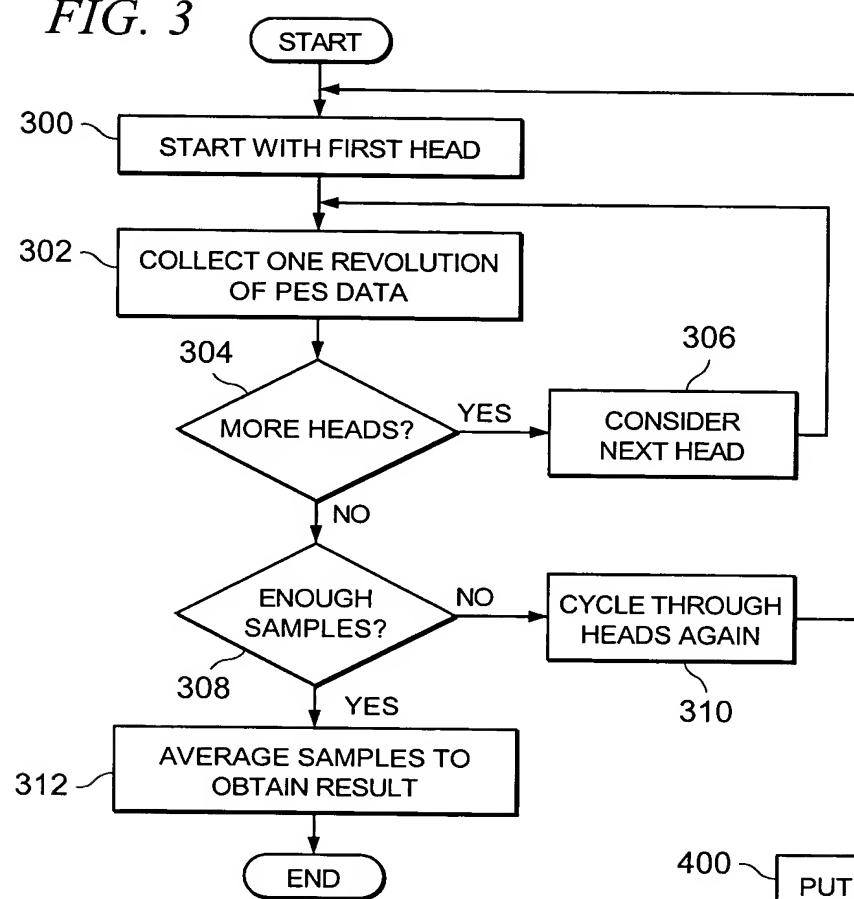


FIG. 4

